Abstract of the Disclosure

A method and apparatus for signaling between devices of a memory system is provided. In accordance with an embodiment of the invention, one or more of several capabilities are implemented to provide heretofore unattainable levels of important system metrics, for example, high performance and/or low cost. These capabilities relate to timing adjustment capabilities, bit time adjustment capabilities, cycle time selection, use of differential and/or non-differential signaling for bus signals and/or clock signals, use of termination structures on a bus, including integrated termination structures, and active control circuitry to allow adjustment to different characteristic bus impedances and power-state control, including a calibration process to optimize the termination value, use of slew rate control circuitry and transfer characteristic control circuitry in the predriver and driver of transmitter blocks to allow adjustment to different characteristic bus impedances and to allow adjustment for other bus properties, including a calibration process to optimize the such circuitry, and/or provision of a memory component designed to prefetch (preaccess) words that are wider than the width of the data bus so that the memory access bandwidth approximately matches the transfer bandwidth, and memory component able to adjust the size of the prefetch (preaccess) word to accommodate connection to data buses of different width.